IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

**[0001]** This application is a continuation of application Serial No. 09/511,609, filed February 23, 2000, ~~pending~~ now U.S. Patent 6,596,565, issued July 22, 2003, which is a divisional of application Serial No. 09/146,945, filed September 3, 1998, now U.S. Patent 6,117,797, issued September 12, 2000.

Please replace paragraph number **[0010]** with the following rewritten paragraph:

**[0010]** In United States Patent 5,450,283 of Lin et al., a method for making a semiconductor device with an exposed die back side is described. The method includes providing a printed wiring board (PWB) substrate with conductive traces, on which a semiconductor die is flip mounted and connected to the conductive traces. An electrically ~~non-~~ nonconductive coupling material is placed between the die and substrate. A package body is formed around the perimeter of the die, covering a portion of the conductive traces and any portion of the coupling material extending beyond the die perimeter. The back side of the die is left exposed through the use of a thin layer of tape placed in the mold cavity prior to the transfer molding of the package body around the die to prevent the flow of molding material forming the package from flowing on the inactive back side of the die. If the thin layer of tape adheres to the die after removal of the semiconductor device from the mold cavity, the thin layer of tape is removed from the die of the semiconductor device.

Please replace paragraph number **[0015]** with the following rewritten paragraph:

**[0015]** In another aspect of the invention, a heat conductive cap is formed over a semiconductor die and comprises a heat sink. A layer of the ~~metal~~ metal-filled gel elastomer is placed between the non-active surface of a die and the cap. Compressing the die into the cap forms the desired adhesion to retain the die within the cap. The compliance of the elastomer enables the die and cap to be pressed together without overpressuring the die/circuit board

interface. In addition, the high thermal conductivity of the elastomer enables devices having a very high heat output to be cooled to temperatures enabling reliable operation.

Please replace paragraph number **[0016]** with the following rewritten paragraph:

**[0016]** The method of the invention includes steps for forming direct die-to-circuit board connections for "heat ~~sinked dice~~" sinked" dice as well as for forming "heat sinked" die modules which may be themselves connected to a substrate such as a circuit board.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

**[0026]** As shown in drawing FIG. 1, a first semiconductor device 10 with a high heat generation rate is shown. The semiconductor device 10 includes a semiconductor die 12 having an active surface 14 with ~~wire~~ bond pads 16, as known in the art. The semiconductor die 12 has a back side 18 which is bonded to a substrate 20, shown here as a printed circuit board (PCB). The ~~wire~~ bond pads 16 are shown as conventionally arrayed near the edges 32 of the semiconductor die 12, and are wire-bonded with conductive, e.g., gold, wires 22 to corresponding electrical connection pads 24 on the substrate 20. Leads on the upper surface 26 and below the upper surface 26 of the substrate 20 are not shown.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

**[0027]** As shown, a heat-conductive heat sink 30 with fins 28 is mounted on the upper, i.e., active surface 14 of the semiconductor die 12, between the rows of ~~wire~~ bond pads 16. The heat sink 30 has a relatively large exposed surface area, enabling a high transfer rate of thermal energy. An adhesive ~~material~~ 34 having a high heat conductance is preferably used, but other adhesives may be alternatively used to bond the heat sink 30 to the semiconductor die 12, particularly because the adhesive ~~material~~ 34 is applied in a very thin layer.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

**[0031]** The heat sink 30 is typically formed of a conductive metal such as aluminum, and has one attachment surface 46 which is attachable by adhesive ~~material~~ 34 to the semiconductor die 12. The heat sink 30 may be of any design which provides the desired heat dissipation, is joinable to the die active surface 14 and sealable by a glob top material 38. For example, the heat sink 30 may either have fins 28 or be finless.

Please replace paragraph number **[0033]** with the following rewritten paragraph:

**[0033]** In drawing FIG. 3A, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally ~~conductive~~ conductive-filled gel elastomer 50 may be either applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. The purpose of the gel elastomer 50 is to provide a protective mask over an area of the semiconductor die 12 to which the heat sink 30 (FIG. 3E) is to be bonded. Alternatively, ~~the elastomer~~ when a second layer is used as a mask, the first layer may be retained on a portion of the semiconductor die 12 after the molding or glob-topping of the semiconductor die 12 for the attachment of a heat sink thereto, if desired (to be described in FIG. 3C). The gel elastomer 50 is applied as a gel or as a semi-solid or solid coupon. The gel elastomer 50, or a suitable silicon elastomeric material, etc. if ~~the~~ the gel elastomer 50 is to be disposed after removal from the semiconductor die 12, or the use of a ~~metal~~ metal-filled gel elastomer ~~50~~ 50, if such is to remain on the semiconductor die 12, may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the gel elastomer 50. The dams 52 may extend along one or more sides of the semiconductor die 12, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. Alternatively, the dams 52 may comprise a second layer of gel elastomer ~~material~~ 50

having a size smaller than that of the gel elastomer ~~material~~ 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the gel elastomer 50 will be later removed by removal of the gel elastomer from the active surface 14 of the semiconductor die 12. Typically, the gel elastomer 50 may be removed simply by peeling it from the active surface 14 of the semiconductor die 12. Typically, if the gel elastomer 50 is to be removed from the semiconductor die 12 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

Please replace paragraph number **[0034]** with the following rewritten paragraph:

**[0034]** The gel elastomer ~~layer~~ 50 is a recently developed material and includes Heat Path™ ~~filled~~ filled cross-linked silicone gels sold by Raychem. As used in this invention, the gel elastomer ~~layer~~ 50 is filled with a conductive material to provide high thermal conductivity. The gel elastomer material is compliant under light pressure, has a solid shape retention, cohesive strength and the ability to wet and adhere to surfaces.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

**[0035]** In the next step, shown in drawing FIG. 3B, the bond pads 16 are ~~wire~~wire bonded to electrical connection pads 24 on the substrate 20 by e.g., thermosonic, thermocompression or ultrasonic methods, as known in the art.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

**[0036]** Alternatively, the wire bonding step may precede application of the gel elastomer ~~layer~~ 50.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

**[0037]** In drawing FIG. 3C, depicted is the next step of the process, that of applying glob top material 38 or suitable potting material to encapsulate the wire connections and the

edges 32 (FIG. 3A) of the semiconductor die 12. The glob top material 38 is typically a thermally resistive polymer such as commercially available epoxy or urethane. The glob top material 38 is typically applied as a curable liquid through a small nozzle, not shown, to extend to the layer of gel elastomer 50, or nearly so. As shown, portions 38A and 38B of the glob top material 38 have spilled onto the exposed surface 44 of gel elastomer ~~layer~~ 50. Without use of the layer of gel elastomer 50, effective removal of glob top portions 38A and 38B may damage the semiconductor die 12 and/or substrate 20 and/or lead wires 22, etc.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

**[0039]** As shown in drawing FIG. 3D, the ~~layer of~~ gel elastomer 50 is then peeled away in direction 42 from the active surface 14 of the semiconductor die 12. It has been found that the lower surface 51 of the gel elastomer ~~layer~~ 50 may be easily and cleanly stripped from the active surface 14 of semiconductor die 12 by simply peeling away the gel elastomer coupon. This leaves the active surface 14 of the semiconductor die 12 clean and prepared for strong bonding of a heat sink 30 with an adhesive ~~material~~ 34, shown in drawing FIG. 3E.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

**[0040]** The particular materials which may be used as die-to-substrate adhesives 40 include those commonly known and/or used in the art. Examples of such are polyimides, a 75% ~~silver~~ silver-filled cyanate ester paste, an 80% ~~silver~~ silver-filled cyanate ester paste, a ~~silver~~ silver-filled lead glass paste, ~~a silver filled cyanate ester paste,~~ etc.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

**[0041]** The adhesive ~~material~~ 34 used to bond the heat sink 30 to the active surface 14 of the semiconductor die 12 may be an epoxy or the above identified die-to-substrate adhesives or an adhesive as known in the art.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

**[0042]** As illustrated in drawing FIG. 3F, further glob top material 48 may be applied to the semiconductor device 10, particularly between the existing glob top material 38 and the heat sink 30, for improved sealing. In this figure, the glob top materials 38 and 48 are shown overcovering the substrate 20 between semiconductor device 10 and an adjacent device, of which only ~~an electrical~~ a connection pad 24A and a bond wire 22A are visible. The semiconductor device 10 is effectively sealed to the substrate 20 to prevent electrical short-circuiting, wire breakage and debonding, and moisture penetration.

Please replace paragraph number **[0043]** with the following rewritten paragraph:

**[0043]** In drawing FIG. 3G, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 (FIG. 4A) of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally ~~conductive~~ conductive-filled gel elastomer 50 is either permanently applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. A layer or piece of disposable elastomer or tape 150 is releasably applied over the gel elastomer 50. The purpose of the elastomer or tape 150 is to provide a protective mask over an area of the gel elastomer 50 attached to the semiconductor die 12 to which the heat sink 30 is to be bonded. The elastomer 150 is applied as a semi-solid or solid coupon. The elastomer 150 is to be disposed after removal from the semiconductor die 12 and may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the elastomer 150. The dams 52 may extend along one or more sides of the elastomer 150, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. Alternatively, the dams 52 may comprise a second layer of ~~gel~~ elastomer 150 having a size smaller than that of the gel elastomer 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38

which lands on the elastomer 150 will be later removed by removal of the elastomer 150 from the surface of the gel elastomer 50. Typically, the elastomer 150 may be removed simply by peeling it from the surface of the gel elastomer 50 permanently attached to the semiconductor die 12. Typically, if the elastomer 150 is to be removed from the gel elastomer 50 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

**[0044]** As shown in drawing FIG. 3G, the layer of elastomer 150 is then peeled away in direction 42 from the surface of the gel elastomer ~~layer~~ 50. It has been found that the lower surface 152 of the elastomer 150 may be easily and cleanly stripped from the surface of the gel elastomer ~~layer~~ 50 by simply peeling away the elastomer coupon. This leaves the surface of the gel elastomer ~~layer~~ 50 clean and prepared for strong bonding of a heat sink 30 with an adhesive ~~material~~ 34, shown in drawing FIG. 3E.

Please replace paragraph number **[0045]** with the following rewritten paragraph:

**[0045]** The glob top materials 38 and 48 may be the same or different materials. Glob top materials useful for this application include HYSOL™ FP4451 material or HYSOL™ FP4450 high purity, low stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc.

Please replace paragraph number **[0046]** with the following rewritten paragraph:

**[0046]** Depicted in drawing FIG. 2 is another aspect of the invention, wherein the semiconductor die 12 is bonded ~~flip~~ flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The semiconductor die 12 has an active surface 14 with a grid of electrical connections 56 attached to the corresponding electrical circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the semiconductor die 12 is directed upwardly, away from the

substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 with adhesive ~~material~~ 34. Glob top material 38 is applied to seal the semiconductor die 12, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30. This type of attachment may similarly be used in chip scale packages, if desired. In such an instance, the semiconductor die 12 would be replaced by a chip scale package bonded ~~flip~~ flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The chip scale package has an active surface 14 with a grid of electrical connections 56 attached to the corresponding electrical circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the chip scale package is directed upwardly, away from the substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 of the chip scale package with adhesive ~~material~~ 34. Glob top material 38 is applied to seal the chip scale package, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30.

Please replace paragraph number **[0048]** with the following rewritten paragraph:

**[0048]** As depicted in drawing FIG. 4A, a flip chip or semiconductor die 12 having an active surface 14 with a grid of electrical connections ~~56~~56, shown as solder ~~balls~~ balls, is down bonded to electrical circuit traces 54 (not shown) on ~~a~~ an upper surface 26 of a substrate 20. The semiconductor die 12 has an opposing back side 18 and edges 32. The substrate 20 may be a printed circuit board (PCB) or other material such as a flex circuit or ceramic. A layer or coupon of thermally ~~conductive~~ conductive-filled gel elastomer 50, ~~alternatively~~ alternatively, a suitable elastomer, silicon elastomeric material, etc. if ~~the~~ the gel elastomer 50 is to be discarded, is

applied as a solid or semisolid to the back side 18 of the semiconductor die 12, either before or (preferably) after the semiconductor die 12 is electrically down bonded to the substrate 20. The gel elastomer 50 masks the back side 18 from glob top material 38 which may be inadvertently misapplied to the back side 18, requiring removal by erosive blasting or other methods. The use of the gel elastomer 50 obviates such glob top removal methods.

Please replace paragraph number **[0052]** with the following rewritten paragraph:

**[0052]** In drawing FIG. 4E, a heat sink 30 is bonded to the back side 18 of semiconductor die 12 by a layer of adhesive ~~material~~ 34, as already ~~described~~ described, relative to the embodiment of drawing FIG. 1.

Please replace paragraph number **[0054]** with the following rewritten paragraph:

**[0054]** Alternatively, a room temperature vulcanizing rubber ~~(RTV)~~ (RTV), which may vary in the degree of thermal conductivity ~~thereof~~ thereof, may be used to completely cover and seal the device to the substrate 20, including the glob top material 38.

Please replace paragraph number **[0060]** with the following rewritten paragraph:

**[0060]** As depicted in drawing FIG. 7, a semiconductor die 12 has an active surface 14 with a ball grid array (BGA) of electrical connections 56 connected to traces (not shown) on a circuit board or other substrate 20 having a plurality of apertures 21 therein. A layer 70 of gel elastomer is then applied to inside attachment surface 46 of a cap style heat sink 30. The heat sink 30 may be finned, or have no fins 28. In one embodiment, the heat sink 30 has resilient spring members 31 having a portion thereof engaging a fin 28 while the other end thereof engages an aperture 21 of the substrate 20 to resiliently retain the heat sink 30 engaging the ~~layer of~~ gel elastomer layer 70 which engages the back side 18 of the semiconductor die 12, leaving the heat sink 30 and semiconductor die 12 free to move with respect to each other.

Please replace paragraph number **[0061]** with the following rewritten paragraph:

**[0061]** In either ~~case~~ case, as illustrated in drawing FIGS. 5, 6, and 7, the back side 18 of semiconductor die 12 is then pressed into the gel elastomer layer 70 for attachment thereto. The adhesion of the gel elastomer layer 70 to the attachment surface 46 of the heat sink 30 and the back side 18 of the semiconductor die 12, as well as the resilient spring members 31, holds the parts in place.

Please replace paragraph number **[0063]** with the following rewritten paragraph:

**[0063]** The embodiment of drawing FIG. 6 is shown with a further ball grid array (BGA) of solder balls 72 on the ~~exterior surface~~ opposite side 58 of the substrate. Thus, the semiconductor device 10 may be bonded to another ~~substrate~~ substrate, such as a circuit board, not shown.